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GATE ARRAY

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[Attached amendments have been incorporated into the text of the translation.]

Claims

A gate array characterized by a construction in which the circuit elements containing a gate circuit possessing a logic function, input buffer, and output buffer are separately formed on the first and second semiconductor substrates so that the amount of heat generated from each chip may be equalized and, while the first and second semiconductor chips described previously are connected by the flip chip packaging method, the second semiconductor chip described previously is tightly attached to the packaging substrate.

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